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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,312	12/15/2003	Naoki Makita	70404.12	1687
54072	7590	10/19/2005		EXAMINER
KEATING & BENNETT, LLP 8180 GREENSBORO DRIVE SUITE 850 MCLEAN, VA 22102				RICHARDS, N DREW
			ART UNIT	PAPER NUMBER
				2815

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,312	MAKITA, NAOKI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 20 July 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-58 is/are pending in the application.
 4a) Of the above claim(s) 38-54 is/are withdrawn from consideration.
 5) Claim(s) 2,3,5,7,9,11,13,18-20,23,26,27,30,31,35-37,57 and 58 is/are allowed.
 6) Claim(s) 1,4,6,8,10,12,14-17,21,22,24,25,28,29,32-34,55 and 56 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 15 December 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 12/15/03.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-3 and 55-58, in the reply filed on 7/20/05 is acknowledged.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 17, 21, 32 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 17 and 21 are indefinite as one of ordinary skill in the art cannot ascertain how "visualizing" the grain boundaries further limits the final structure of the claimed device. These claims include a method step of visualizing through an etching process using a Secco etching method. It is unclear as to whether these claims include some further structural limitation as the result of performing an etching process or whether

they merely require that the device be able to be etched using a Secco etching method to allow visualization of the grain boundaries.

Claims 32 and 33 are indefinite as it is not well understood what structure is covered by the "domain diameters or crystal domains" so that one could ascertain if a given structure infringed upon these claims or not. The crystal grains themselves as disclosed in applicant's specification as having diameters of about 100 to 1000 nm. Thus, the 2 to 10 micron "domain diameters" are not well understood. How is the "domain diameter" different from the crystal grain diameter?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 4, 6, 8, 10, 14-17, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. (US 2002/0102823 A1).

Yamaguchi et al. disclose in figure 4 a semiconductor device comprising a thin film transistor including a semiconductor layer 9 (labeled in figures 2 and 3, unlabeled in figure 4) that includes a channel region 13 (on left side), a source region and a drain

region 14, a gate insulating film 5 provided on the semiconductor layer, and a gate electrode 6 for controlling a conductivity of the channel region, wherein a surface of the semiconductor layer includes a protruding portion, and a side inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer. As shown, the gate electrode has a side inclination angle of approximately 90 degrees.

With regard to claim 4, as seen in figure 4 Yamaguchi et al. disclose multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees.

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as disclosed in paragraph [0076] an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 14, the semiconductor film is a crystalline film and the protruding portions are located over crystal grain boundaries.

With regard to claim 15, as can be seen in figures 3 and 4, the crystal grain boundary is a multipoint where three or more crystal grains meet.

With regard to claim 16, the diameter of the crystal grains is about 100 to about 1000 nm.

With regard to claim 17, the crystal grains are capable of being visualized through a Secco etching method.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claims 28 and 29, the semiconductor layer is made up primarily of regions oriented along <111> crystal zone planes wherein 50% or more of the regions are oriented along a (110) plane.

With regard to claims 55 and 56, Yamaguchi et al. disclose an electronic device comprising the device of claim 1 and further disclose a display section where an image is displayed by using the semiconductor device (see figure 5).

7. Claims 1, 4, 6, 8, 10, 22, 34, 55 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (US Patent No. 5,693,959).

Inoue et al. disclose in figure 1, for example, a thin film transistors as claimed in claim 1. Inoue et al. disclose a semiconductor layer having protruding portions (under contacts 106a/106b) where a side inclination angle of the gate 104 is greater than an inclination angle of the protruding portions.

With regard to claim 4, Inoue et al. disclose multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees.

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as disclosed in column 6 lines 46-48 an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claim 34, Inoue et al. disclose a lightly-doped impurity region 102b/102f at a junction between the channel and the source or drain region.

With regard to claims 55 and 56, Inoue et al. disclose an electronic device comprising the device of claim 1 and further disclose a display section where an image is displayed by using the semiconductor device (see figures 7 or 8 for example).

8. Claims 1, 4, 6, 12 and 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi et al. (US 2003/0080384 A1).

Takahashi et al. disclose in figure 5(c) a semiconductor device including a thin film transistor including a semiconductor layer 71 that has a protruding portion, an insulator 69, a gate 70, a source and drain 66, where an inclination angle of the gate is greater than an inclination angle of the protruding portion.

With regard to claim 4, Takahashi et al. disclose multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees.

With regard to claim 12, an average surface roughness of the surface of the semiconductor layer is about 4 to about 30 nm.

With regard to claim 55, Takahashi et al. disclose an electronic device comprising the device of claim 1.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. as applied to claims 1, 4, 6, 8, 10, 14-17, 22, 28, 29, 55 and 56 above, and further in view of Yamazaki et al. (US 2002/0100937 A1).

Yamaguchi et al. teach forming their layer using a melting/solidification process but do not teach including a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

Yamazaki et al. teach adding a catalyst element to a semiconductor film to promote crystallization during a melting/solidification process.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include a catalyst element in the semiconductor layer of Yamaguchi in order to promote crystallization to form a crystalline layer having excellent crystallinity.

With regard to claim 25, Yamazaki teach that the catalyst element is nickel (Ni).

Allowable Subject Matter

11. Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35, 36, 37, 57 and 58 are allowed.

12. The following is an examiner's statement of reasons for allowance: Prior art of record fails to teach, disclose, or suggest, either alone or in combination, the device as recited in claim 2 including a gate electrode includes a first step portion and a second step portion provided on the first step portion, and a side surface inclination angle of each of the first and second step portions is larger than an inclination angle of the protruding portion of the semiconductor layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamazaki et al. (US 2002/0127827 A1), Sakakura et al. (US 2003/0038321 A1)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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